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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10039852	FILING DATE 10/22/2001	CLASS 714	SUBCLASS 738	GAU 2133	EXAMINER <i>Hj...</i>
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RSC

TRIMMING

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
TAIWAN 90107334 03/28/2001

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		JCLA7022
Verified and Acknowledged Examiners's initials		
TITLE : Method and circuit for testing a chip		

U.S. DEPT. OF COMMERCE / PAT. & TM. PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner PREPARED FOR ISSUE Application Examiner	
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